1. An electromagnetic element comprising:

a substrate with at least a first and second through-holes that define between them a coil winding area that includes a top surface of said substrate, a bottom surface of said substrate, and side surfaces of said through-holes;

a first layer of magnetic material provided on said substrate in said coil winding area; and

a first layer of electrically conductive material forming at least one coil winding provided on said substrate in said coil winding area.

2. The electromagnetic element of claim 1, wherein said conductive material is copper or an alloy of copper.

3. The electromagnetic element of claim 1, wherein said conductive material is aluminum or an alloy of aluminum.

4. The electromagnetic element of claim 1, wherein said first layer of electrically conductive material forms two coil windings.

5. The electromagnetic element of claim 4, wherein said electromagnetic element is a transformer and said two coil windings form the primary and secondary coil windings of said transformer.

6. The electromagnetic element of claim 1 further comprising a first insulating layer between said substrate and said first layer of magnetic material.

7. The electromagnetic element of claim 6, wherein said first insulating layer is formed of a high temperature polymer film.

8. The electromagnetic element of claim 7, wherein said high temperature polymer film is a polyimide.

9. The electromagnetic element of claim 6, wherein said first insulating layer is formed of an oxide or a nitride.

10. The electromagnetic element of claim 6, wherein said first insulating layer has a thickness of 0.5 to 1 μm.

11. The electromagnetic element of claim 1, wherein said first layer of magnetic material is made of Fe –X –N alloy or Fe –X—B—N alloy, wherein X is at least one atom selected from the group consisting of Zr, Hf, Ti, Nb, Ta, V, Mo, W, and Cr.

12. The electromagnetic element of claim 11, wherein said first layer of magnetic material is further formed of a plurality of thin soft magnetic

layers and at least one insulating spacer layer formed between said thin soft magnetic layers.

13. The electromagnetic element of claim 12, wherein said insulating spacer layer is formed of a material selected form the group consisting of Permalloy (NiFe), NiFeMo, Co-Zr, CoZrRe, CoFeSiB, CoNbZr, and Co-Cr-O granular films.

14. The electromagnetic element of claim 6 further comprising a second insulating layer between said first layer of magnetic material and said first layer of electrically conductive material.

15. The electromagnetic element of claim 14, wherein said second insulating layer is formed of a high temperature polymer film.

16. The electromagnetic element of claim 15, wherein said high temperature polymer film is a polyimide.

17. The electromagnetic element of claim 14, wherein said second insulating layer is formed of an oxide or a nitride.

18. The electromagnetic element of claim 14, wherein said second insulating layer has a thickness of 0.5 to 1 μm.

19. The electromagnetic element of claim 14 further comprising a top protective insulating layer over said first layer of electrically conductive material.

20. The electromagnetic element of claim 19 further comprising a passivating layer over said top protective insulating layer.

21. The electromagnetic element of claim 14 further comprising a second layer of magnetic material formed over said first layer of electrically conductive material.

22. The electromagnetic element of claim 1, wherein said second layer of magnetic material is made of Fe –X –N alloy or Fe –X—B—N alloy, wherein X is at least one atom selected from the group consisting of Zr, Hf, Ti, Nb, Ta, V, Mo, W, and Cr.

23. The electromagnetic element of claim 22, wherein said second layer of magnetic material is further formed of a plurality of thin soft magnetic layers and at least one insulating spacer layer formed between said thin soft magnetic layers.

24. The electromagnetic element of claim 23, wherein said insulating spacer layer is formed of a material selected form the group consisting

of Permalloy (NiFe), NiFeMo, Co-Zr, CoZrRe, CoFeSiB, CoNbZr, and Co-Cr-O granular films.

25. The electromagnetic element of claim 21 further comprising a third insulating layer between said first layer of electrically conductive material and said second layer of magnetic material.

26. The electromagnetic element of claim 25, wherein said third insulating layer is formed of a high temperature polymer film.

27. The electromagnetic element of claim 26, wherein said high temperature polymer film is a polyimide.

28. The electromagnetic element of claim 25, wherein said third insulating layer is formed of an oxide or a nitride.

29. The electromagnetic element of claim 25, wherein said third insulating layer has a thickness of 0.5 to 1 μm.

30. The electromagnetic element of claim 25 further comprising a second layer of electrically conductive material forming at least one coil on said second layer of magnetic material.

31. The electromagnetic element of claim 30 further comprising an insulating layer between said second layer of magnetic material and said second layer of electrically conductive material.

32. The electromagnetic element of claim 30 wherein said second layer of conductive material is copper or an alloy of copper.

33. The electromagnetic element of claim 30 wherein said second layer of conductive material is aluminum or an alloy of aluminum.

34. The electromagnetic element of claim 30, wherein said second layer of electrically conductive material forms two coils.

35. The electromagnetic element of claim 30 further comprising a top protective insulating layer over said second layer of electrically conductive material.

36. The electromagnetic element of claim 35 further comprising a passivating layer over said top protective insulating layer.

37. The electromagnetic element of claim 1, wherein said substrate is a semiconductor substrate.

38. The electromagnetic element of claim 37, wherein said semiconductor substrate is a silicon substrate.

39. The electromagnetic element of claim 37, wherein said semiconductor substrate is a germanium substrate.

40. The electromagnetic element of claim 37, wherein said semiconductor substrate is a gallium arsenide substrate.

41. The electromagnetic element of claim 1, wherein said substrate is a quartz substrate.

42. The electromagnetic element of claim 1, wherein said substrate is a ceramic substrate.

43. The electromagnetic element of claim 1, wherein said substrate is a Al_2O_3/TiC substrate.

44. The electromagnetic element of claim 1, wherein said electromagnetic element is selected from the group consisting of a microtransformer and a microinductor.

45. The electromagnetic element of claim 1, wherein said semiconductor substrate further contains circuitry for a DC-DC converter.

46. The electromagnetic element of claim 45, wherein said semiconductor substrate further contains circuitry for a power supply which includes said DC-DC converter.

47. A method for fabricating a microtransformer comprising the steps of:

providing a substrate with at least a first and second through-holes that define between them a coil winding area that includes a top surface of said substrate, a bottom surface of said substrate, and side surfaces of said through-holes;

forming a first layer of magnetic material on said substrate in said coil winding area; and

forming a first layer of electrically conductive material forming at least one coil winding on said substrate in said coil winding area.

48. The method of claim 47, wherein said first layer of electrically conductive material has two coils.

49. The method of claim 47 further comprising the step of providing a first insulating layer between said first layer of magnetic material and said substrate.

50. The method of claim 49 further comprising the step of providing a second insulating layer between said first layer of magnetic material and said layer of electrically conductive material.

51. The method of claim 50 further comprising the step of providing a top protective insulating layer over said first layer of electrically conductive material.

52. The method of claim 51 further comprising the step of providing a passivating layer over said top protective insulating layer.

53. The method of claim 50 further comprising the step of forming a second layer of magnetic material over said first layer of electrically conductive material.

54. The method of claim 53 further comprising the step of providing a third insulating layer between said first layer of electrically conductive material and said second layer of magnetic material.

55. The method of claim 54 further comprising the step of forming a second layer of electrically conductive material forming at least one coil on said second layer of magnetic material.

56. The method of claim 55 further comprising the step of forming an insulating layer between said second layer of magnetic material and said second layer of electrically conductive material.

57. The method of claim 55 further comprising the step of providing a top protective insulating layer over said second layer of electrically conductive material.

58. The method of claim 57 further comprising the step of providing a passivating layer over said top protective insulating layer.

59. A system-on-chip comprising:

a substrate having a through-hole microtransformer formed thereon; and

at least one integrated circuit chip attached to said substrate and electrically connected to said substrate.

60. The system-on-chip of claim 59, wherein said through-holes microtransformer is formed in a coil winding area defined by first and second through-holes in said substrate, said coil winding area including a top surface of said substrate, a bottom surface of said substrate, and side surfaces of said through-holes.

61. The system-on-chip of claim 59, wherein said microtransformer further comprises a first layer of magnetic material provided on said substrate in said coil winding area and a first layer of electrically conductive material forming at least one coil winding provided on said substrate in said coil winding area.

62. The system-on-chip of claim 61, wherein said layer of electrically conductive material forms two coil windings.

63. The system-on-chip of claim 62, wherein said two coil windings form a primary and secondary coil windings of said microtransformer.

64. The system-on-chip of claim 61, wherein said microtransformer further comprises a first insulating layer between said substrate and said first layer of magnetic material.

65. The system-on-chip of claim 64, wherein said microtransformer further comprises a second insulating layer formed between said first layer of magnetic material and said first layer of electrically conductive material.

66. The system-on-chip of claim 65, wherein said microtransformer further comprises a top protective insulating layer over said first layer of electrically conductive material.

67. The system-on-chip of claim 66, wherein said microtransformer further comprises a passivating layer over said top protective insulating layer.

68. The system-on-chip of claim 65, wherein said microtransformer further comprises a second layer of magnetic material formed over said first layer of electrically conductive material.

69. The system-on-chip of claim 68, wherein said microtransformer further comprises a third insulating layer between said first layer of electrically conductive material and said second layer of magnetic material.

70. The system-on-chip of claim 69, wherein said microtransformer further comprises a second layer of electrically conductive material forming at least one coil on said second layer of magnetic material.

71. The system-on-chip of claim 70, wherein said microtransformer further comprises an insulating layer between said second layer of magnetic material and said second layer of electrically conductive material.

72. The system-on-chip of claim 71, wherein said microtransformer further comprises a top protective insulating layer over said second layer of electrically conductive material.

73. The system-on-chip of claim 72, wherein said microtransformer further comprises a passivating layer over said top protective insulating layer.

74. The system-on-chip of claim 59, wherein said at least one chip contains analog circuitry.

75. The system-on-chip of claim 59, wherein said at least one chip contains digital circuitry.

76. The system-on-chip of claim 59 further comprising a power supply on said substrate.

77. The system-on-chip of claim 59 further comprising a DC-DC converter on said substrate.

78. The system-on-chip of claim 59, wherein said substrate is a semiconductor substrate.

79. The system-on-chip of claim 78, wherein said semiconductor substrate is a silicon substrate.

80. The system-on-chip of claim 78, wherein said semiconductor substrate is a germanium substrate.

81. The system-on-chip of claim 78, wherein said semiconductor substrate is a gallium arsenide substrate.

82. The system-on-chip of claim 59, wherein said substrate is a quartz substrate.

83. The system-on-chip of claim 59, wherein said substrate is a ceramic substrate.

84. The system-on-chip of claim 59, wherein said substrate is a Al_2O_3/TiC substrate.

85. A processor-based system, comprising:

a processor; and

an integrated circuit coupled to said processor, said integrated circuit including a through-hole microtransformer, said microtransformer being formed in a coil winding area defined by a first and second through-holes in a

substrate, said coil winding area including a top surface of said substrate, a bottom surface of said substrate, and side surfaces of said through-holes.

86. The processor-based system of claim 85, wherein said microtransformer further comprises a first layer of magnetic material provided on said substrate in said coil winding area and a first layer of electrically conductive material forming at least one coil winding provided on said substrate in said coil winding area.

87. The processor-based system of claim 86, wherein said microtransformer further comprises a first insulating layer formed between said substrate and said first layer of magnetic material.

88. The processor-based system of claim 87, wherein said microtransformer further comprises a second insulating layer formed between said first layer of magnetic material and said first layer of electrically conductive material.

89. The processor-based system of claim 88, wherein said microtransformer further comprises a top protective insulating layer over said first layer of electrically conductive material.

90. The processor-based system of claim 89, wherein said microtransformer further comprises a passivating layer over said top protective insulating layer.

91. The processor-based system of claim 88, wherein said microtransformer further comprises a second layer of magnetic material formed over said first layer of electrically conductive material.

92. The processor-based system of claim 91, wherein said microtransformer further comprises a third insulating layer between said first layer of electrically conductive material and said second layer of magnetic material.

93. The processor-based system of claim 92, wherein said microtransformer further comprises a second layer of electrically conductive material forming at least one coil on said second layer of magnetic material.

94. The processor-based system of claim 93, wherein said microtransformer further comprises an insulating layer between said second layer of magnetic material and said second layer of electrically conductive material.

95. The processor-based system of claim 94, wherein said microtransformer further comprises a top protective insulating layer over said second layer of electrically conductive material.

96. The processor-based system of claim 95, wherein said microtransformer further comprises a passivating layer over said top protective insulating layer.

97. The processor-based system of claim 85, wherein said integrated circuit is part of a memory circuit.

98. The processor-based system of claim 85, wherein said substrate is a semiconductor substrate.

99. The processor-based system of claim 98, wherein said semiconductor substrate is a silicon substrate.

100. The processor-based system of claim 98, wherein said semiconductor substrate is a germanium substrate.

101. The processor-based system of claim 98, wherein said semiconductor substrate is a gallium arsenide substrate.

102. The processor-based system of claim 85, wherein said substrate is a quartz substrate.

103. The processor-based system of claim 85, wherein said substrate is a ceramic substrate.

104. The processor-based system of claim 85, wherein said substrate is a Al_2O_3/TiC substrate.